**WHAT IS CLAIMED IS:**

1. A computer system comprising:

a processor;

a plurality of input/output (I/O) nodes serially coupled to the processor through a plurality of packet bus links, wherein each of the plurality of I/O nodes includes an upstream packet bus interface, a downstream packet bus interface, a peripheral bus interface, and an I/O tunnel; and

a peripheral bus coupled to the peripheral bus interface of one of the plurality of I/O nodes;

wherein the one of the plurality of I/O nodes is configured, in a first mode, to selectively convey packets through the I/O tunnel between the upstream packet bus interface and the downstream packet bus interface and to selectively convey particular packets from the upstream packet bus interface to the peripheral bus interface, and in a second mode, to replicate electrical signals corresponding to packets passing through the I/O tunnel on the peripheral bus.

2. The computer system as recited in claim 1, wherein in the first mode, the computer system is configured to generate cycles on a peripheral bus in response to the particular packets being selectively conveyed from the upstream packet bus interface to the peripheral bus interface.

3. The computer system as recited in claim 1, wherein the peripheral bus includes a peripheral bus connector.

4. The computer system as recited in claim 3 further comprising a dummy card, wherein the dummy card is configured to be inserted into the peripheral bus

connector, and wherein the dummy card is further configured to be coupled to a signal analyzer.

5. The computer system as recited in claim 4, wherein the signal analyzer is a logic analyzer.

6. The computer system as recited in claim 3, further comprising a signal analyzer card, wherein the signal analyzer card is configured to be inserted into the peripheral bus connector.

7. The computer system as recited in claim 1, wherein the computer system is configured for performing upstream packet transactions and downstream packet transactions, wherein downstream packet transactions originate at the processor, and wherein upstream packet transactions terminate at the processor.

8. The computer system as recited in claim 7, wherein the I/O node is further configured to, in the second mode, to provide an indication of whether a given packet for which electrical signals are replicated is being conveyed upstream or downstream.

9. The computer system as recited in claim 1, wherein in the I/O node includes an arbitration unit, wherein, in the second mode, the arbitration unit is configured to determine the order in which electrical signals from a first packet will be replicated relative to electrical signals from a second packet.

10. The computer system as recited 1, wherein the I/O node includes a command register, wherein the command register is configured to store one or more bits

indicative of whether the I/O node is operating in the first mode or the second mode.

11. The computer system as recited in claim 10, wherein the I/O node is configured to enter the second mode responsive to inputting one or more signals corresponding to the one or more bits into the command register.

12. The computer system as recited in claim 11, wherein said inputting is performed during a power-on reset.

13. The computer system as recited in claim 1, wherein the peripheral bus is a peripheral component interconnect (PCI) bus.

14. The computer system as recited in claim 1, wherein the peripheral bus is an advanced graphics port (AGP) bus.

15. The computer system as recited in claim 1, wherein the peripheral bus is a general-purpose instrument bus (GPIB).

16. The computer system as recited in claim 1, wherein the electrical signals are replicated onto one or more signal lines of the peripheral bus.

17. The computer system as recited in claim 1, wherein the peripheral bus interface is configured, in the first mode, to convey packets into the I/O tunnel.

18. An input/output (I/O) node comprising:
an upstream packet bus interface and a downstream packet bus interface;
a peripheral bus interface configured to be coupled to a peripheral bus; and

an I/O tunnel;

wherein the I/O node is configured, in a first mode, to selectively convey packets through the I/O tunnel between the upstream packet bus interface and the downstream packet bus interface and to selectively convey particular packets from the upstream packet bus interface to the peripheral bus interface, and in a second mode, to replicate electrical signals corresponding to packets passing through the I/O tunnel on the peripheral bus.

19. The I/O node as recited in claim 18, wherein the peripheral interface unit is configured to generate cycles on the peripheral bus in response to the particular packets being selectively conveyed from the upstream packet bus interface to the peripheral bus interface.

20. The I/O node as recited in claim 18, wherein the upstream packet bus interface and the downstream packet bus interface are each configured to be coupled to a packet bus link.

21. The I/O node as recited in claim 20, wherein the I/O node is configured to perform upstream packet transactions and downstream packet transactions.

22. The I/O node as recited in claim 21, wherein the I/O node is further configured to provide an indication as to whether a given packet is being conveyed upstream or downstream.

23. The I/O node as recited in claim 18, wherein the I/O node includes an arbitration unit, wherein, in the second mode, the arbitration unit is configured to determine

the order in which electrical signals from a first packet will be replicated relative to electrical signals from a second packet.

24. The I/O node as recited in claim 18, wherein the I/O node includes a command register, wherein the command register is configured to store one or more bits indicative of whether the I/O node is operating in the first mode or the second mode.

25. The I/O node as recited in claim 24, wherein the I/O node is configured to enter the second mode responsive to inputting one or more signals corresponding to the one or more bits in the command register.

26. The I/O node as recited in claim 25, wherein said inputting is performed during a power on reset.

27. The I/O node as recited in claim 18, wherein the peripheral bus interface is configured, in the first mode, to convey packets into the I/O tunnel.

28. A method for observing transactions on a packet bus in a computer system, the method comprising:

operating an input/output (I/O) node in an analysis mode, wherein the I/O node includes:

an upstream packet bus interface and a downstream packet bus interface;

a peripheral bus interface configured to be coupled to a peripheral bus; and

an I/O tunnel;

wherein the I/O node is configured, in a normal mode, to selectively convey packets through the I/O tunnel between the upstream packet bus interface and the downstream packet bus interface and

to selectively convey particular packets from the upstream packet bus interface to the peripheral bus interface, and in the analysis mode, to replicate electrical signals corresponding to packets passing through the I/O tunnel on the peripheral bus;

coupling a signal analyzer to a peripheral bus, wherein the peripheral bus is coupled to the peripheral bus interface; and

observing the electrical signals replicated on the peripheral bus.

29. The method as recited in claim 28, wherein, in the normal mode, the computer system is configured to generate cycles on a peripheral bus in response to the particular packets being selectively conveyed from the upstream packet bus interface to the peripheral bus interface.

30. The method as recited in claim 28, wherein the peripheral bus includes a peripheral bus connector.

31. The method as recited in claim 30, wherein a dummy card is coupled to the peripheral bus connector.

32. The method as recited in claim 31, wherein the signal analyzer is coupled the dummy card.

33. The method as recited in claim 32, wherein the signal analyzer is a logic analyzer.

34. The method as recited in claim 30, wherein a signal analyzer card is coupled to the peripheral bus connector.

35. The method as recited in claim 34, wherein the signal analyzer card is a logic analyzer card.

36. The method as recited in claim 28, wherein the computer system includes a processor, and a plurality of I/O nodes serially coupled to the processor.

37. The method as recited in claim 36, wherein the computer system is configured for upstream transactions and downstream transactions, wherein downstream transactions originate at the processor, and wherein upstream transactions terminate at the processor.

38. The method as recited in claim 37 further comprising providing an indication of whether the electrical signals correspond to packets conveyed in an upstream transaction or a downstream transaction.

39. The method as recited in claim 28, wherein the I/O node includes a command register, wherein the command register is configured to store one or more bits indicative of whether the I/O node is operating in the normal mode or the analysis mode.

40. The method as recited in claim 39, wherein the I/O node is configured to enter the analysis mode responsive to inputting one or more signals corresponding to the one or more bits into the command register.

41. The method as recited in claim 40, wherein said inputting is performed during a power on reset.

42. The method as recited in claim 28 further comprising replicating the signals onto one or more signal lines of the peripheral bus.

43. The method as recited in claim 28, wherein the I/O node includes an arbitration unit, wherein, in the analysis mode, the arbitration unit is configured to determine the order in which electrical signals from a first packet will be replicated relative to electrical signals from a second packet.

44. The method as recited in claim 28, wherein the peripheral bus is a peripheral component interconnect (PCI) bus.

45. The method as recited in claim 28, wherein the peripheral bus is an advanced graphics port (AGP) bus.

46. The method as recited in claim 28, wherein the peripheral bus is a general purpose instrument bus (GPIB).

47. The method as recited in claim 28, wherein the wherein the peripheral bus interface is configured, in the first mode, to convey packets into the I/O tunnel.